IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Eliyahou Harari et al.		
Title:	Flash EEPROM System		
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APPELLANT'S BRIEF UNDER 37 C.F.R. 41.37
ON APPEAL TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

In response to the Notice of Non-Compliant Appeal Brief filed in this application that was mailed on November 19, 2007, Applicants submit this revised Appeal Brief.

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I. REAL PARTY IN INTEREST

The real party in interest is SanDisk Corporation, a corporation of the state of Delaware, the assignee of all right, title and interest in the present patent application from the inventors, Eliyahou Harari, Robert D. Norman, and Sanjay Mehrotra.

II. RELATED APPEALS AND INTERFERENCES

Several applications that share disclosure with the present application, all similarly claiming priority from, and limited to the matter disclosed in, US patent application number 07/337,566, have been involved in an appeal, interference, or judicial proceeding. Although they may not have a direct bearing on the present appeal, the following list is provided here through an abundance of caution:

US patent application number 09/103,056 has been involved in Patent Interference No. 104,760. The decision from this Interference is included in the Related Proceedings Appendix.

US patent application number 09/056,398 has been involved in an Appeal. The decision from this Appeal is included in the Related Proceedings Appendix.

A Notice of Appeal and Appeal brief were filed in US patent application number 10/417,954, but the appeal did not go forward and the examiner reopened prosecution. Consequently, there is no decision and the inclusion of one is *not applicable*.

An appeal is currently pending in US patent application number 09/114,504. Consequently, there is as yet no decision and the inclusion of one is *not applicable*.

An appeal is currently pending in US patent application number 09/143,233.. Consequently, there is as yet no decision and the inclusion of one is *not applicable*.

US patent number 5,418,752 has been involved in a U.S. International Trade Commission action, Investigation No. 337-TA-382. The decision from this action is included in the Related Proceedings Appendix.

US patent number 5,991,517 has been involved in a U.S. International Trade Commission action, Investigation No. 337-TA-560. The decision from this action is included in the Related Proceedings Appendix.

US patent number 5,602,987 has been involved in litigation, *SanDisk Corporation v. Lexar Media, Inc.*, United States District Court for Northern California, San Francisco Division, Case No. C98-0111 CRB (PJH). This case was settled. Consequently, there is no decision and the inclusion of one is *not applicable*.

US patent number 5,602,987 is involved in pending litigation. The decision from an appeal in this case, *SanDisk Corporation v. Memorex Products, Inc.*, 415 F.3d 1278, 75USPQ 2D1475 (Fed. Cir. 2005), is included in the Related Proceedings Appendix.

US patent number 5,719,808 is involved in pending litigation, *STMicroelctronics, Inc. v. SanDisk Corporation v. STMicroelctronics, Inc.*, United States District Court for the Eastern District of Texas, Sherman Division, Case Action No. 4:05CV45. Consequently, there is as yet no decision and the inclusion of one is *not applicable*.

III. STATUS OF THE CLAIMS

The subject application is a continuation of patent application serial no. 09/280,385, filed March 3, 1999, now abandoned, which is a continuation of patent application serial no. 08/771,708, filed December 20, 1996, now patent no. 5,991,517, which is a continuation of patent application serial no. 08/174,768, filed December 29, 1993, now patent no. 5,602,987, which is a continuation of patent application serial no. 07/963,838, filed October 20, 1992, now patent no. 5,297,148, which in turn is a division of patent application serial no. 07/337,566, filed April 13, 1989, abandoned. The original parent application claims 1-62 were cancelled in a Preliminary Amendment filed concurrently with the subject application on November 30, 2001. This Preliminary Amendment also added claims 63-97, which were, respectively, copies of claims 1-3, 5, 7-9, 14-16, 18, 20-21, 25-27, 31-35, 37, 39-46, 48 and 50-53 of U.S. patent no. 6,141,267 - Kirihata *et al.* granted October 31, 2000.

In the first Office Action on the merits (January 31, 2003), claims 63-97 were rejected under 35 U.S.C.112, first paragraph, for the written description requirement due to a number of elements. A Response (mailed April 25, 2003) to the first Office Action argued that the 35 U.S.C. 112, first paragraph, rejections were not well founded and that the written description requirement was met. A second Office Action (July 30, 2003) rejecting claims 63-97 was based on new grounds, but again under 35 U.S.C.112, first paragraph, for failing to comply with the

written description for "a memory array comprising a plurality of groups of ... address cells, said cells in each of said groups of ... address cells ... storing ... addresses". A Response (mailed September 24, 2003) to the second Office Action argued that the 35 U.S.C. 112, first paragraph, rejection was not well founded and that the written description requirement was met. Three more Office Actions on the same basis followed, with a Response in reply to each arguing that the 35 U.S.C. 112, first paragraph, rejection was not well founded and that the written description requirement was met. In an attempt to try and clarify the bases of these rejections, the Response to the fifth Office Action (and the fourth on the same basis) added claims 98-103, which are similar to, and correspond to, the previously pending independent claims, but having some what differing language. The most recent Office Action (mailed May 19, 2005) extended to previous basis of rejection to these newly added claims as well.

Claims 63-103 stand rejected under 35 U.S.C. §112, first paragraph, as the Applicants allegedly failed to comply with the written description for "a memory array comprising a plurality of groups of ... address cells, said cells in each of said groups of ... address cells ... storing ... addresses".

Claims 1-62 have been cancelled.

IV. STATUS OF AMENDMENTS

On November 17, 2005, a Notice of Appeal from the Examiner's decision rejecting claims 63-103 was filed. No Amendments have been filed since the May 19, 2005, mailing date of the Office Action from which this Appeal is being taken.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

As background, this section gives a summary of the present invention. Since the claims stand rejected under the written description requirement of 35 U.S.C. §112, first paragraph, some of this material is presented in more detail below in section VII in order to demonstrate that adequate description is supplied in the specification of the subject application.

The claimed subject matter is a memory system and method of operating it for managing defects in a memory array. The memory array includes two sets of groups of memory cells, the first of these groups for the storing of data and the other of these groups for storing addresses.

When one or more of these groups of cells are accessed, to read the data content for example, the memory determines whether an inputted address matches one of these groups. If such an address match condition is detected, the corresponding data from the accessed group is output.

The pending independent claims are claims 63, 82, 85, 87, 89, 91, 96, and 98-103. Claim 98 will be used as the exemplary claim:

> 98. A defect management engine comprising:
> a memory array comprising a plurality of groups of first cells and second cells, said cells in each of said groups of first cells and second cells respectively storing data and addresses;
> means for accessing at least one of said plurality of groups of first cells and second cells;
> means for detecting an address match condition for each of said accessed groups, wherein the address of said accessed group matches an inputted address; and
> means for outputting data from said accessed group of first cells when said address match condition is detected.

The present patent application primarily describes this subject matter in the "Defect Mapping" section that begins on line 12 of page 14 of the specification. The various access, detection, and output circuit are shown for a read process in Figure 6, which is primarily described beginning on page 17, line 26. Many of the independent claims use means plus function language, such as in claim 98, for example. The "means for accessing ..." can be taken to include elements 503, 511, and 513 of Figure 6, described between page 17, line 16, to page 18, line 28. The "means for detecting an address match condition ..." can be taken to include elements 509 and 521 as described on page 19, lines 17-22. The "means for outputting data ..." can be taken to include elements 515, 517, 519, and 525 of Figure 6, described between page 18, line 18, to page 20, line 2.

The groups of memory cells storing data and addresses, whose alleged lack of description is the sole issue in this appeal, are shown in Figure 5. This figure shows an exemplary partition of memory sectors according to the present application. Figure 5 is primarily described beginning at line 23 of page 16. According to this sector partition, the sectors include a first group of memory cells, 403 "DATA", that store data and a second group of memory cells, 409 "DEFECT MAP", that store the addresses of defective cells and backup cells.

Each of the independent claims will now explicitly be mapped onto the application. Beginning with claim 63, where the "first cells" and "second cells" are, respectively, "data cells" and "address cells":

63. A defect management engine comprising:

a memory array comprising a plurality of groups of data cells and address cells, said cells in each of said groups of data cells and address cells respectively storing data and addresses;

means for accessing at least one of said plurality of groups of data cells and address cells;

means for detecting an address match condition for each of said accessed groups, wherein the address of said accessed group matches an inputted address; and

means for outputting data from said accessed group of data cells when said address match condition is detected.

The present patent application primarily describes this subject matter in the "Defect Mapping" section that begins on line 12 of page 14 of the specification. The various access, detection, and output circuit are shown for a read process in Figure 6, which is primarily described beginning on page 17, line 26. The "means for accessing ..." can be taken to include elements 503, 511, and 513 of Figure 6, described between page 17, line 16, to page 18, line 28. The "means for detecting an address match condition ..." can be taken to include elements 509 and 521 as described on page 19, lines 17-22. The "means for outputting data ..." can be taken to include elements 515, 517, 519, and 525 of Figure 6, described between page 18, line 18, to page 20, line 2. The groups of memory cells storing data and addresses are shown in Figure 5. This figure shows an exemplary partition of memory sectors according to the present application. Figure 5 is primarily described beginning at line 23 of page 16. According to this sector partition, the sectors include a group of memory cells, 403 "DATA", that store data and a group of memory cells, 409 "DEFECT MAP", that store the addresses of defective cells and backup cells.

Claim 82 differs from claim 63 in that the defect management engine in coupled to "at least on main memory" and in that the "address cells" and "memory cells" are "redundancy address cells" and "redundancy memory cells":

82. A defect management engine coupled to at least one main memory comprising:

a memory array comprising a plurality of groups of redundancy data cells and redundancy address cells, said cells in each of said groups of redundancy data cells and redundancy address cells respectively storing redundancy data and redundancy addresses;

means for accessing at least one of said plurality of groups of redundancy data cells and redundancy address cells;

means for detecting a redundancy address match condition for each of said accessed groups, wherein the redundancy address of said accessed group matches one of a plurality of inputted addresses; and

means for outputting redundancy data from said accessed group of redundancy data cells and redundancy address cells when said redundancy address match condition is detected.

The present patent application primarily describes this subject matter in the "Defect Mapping" section that begins on line 12 of page 14 of the specification. The defect management engine is part of controller 31 in Figure 6, with the memory as 33. The various access, detection, and output circuit are shown for a read process in Figure 6, which is primarily described beginning on page 17, line 26. The "means for accessing ..." can be taken to include elements 503, 511, and 513 of Figure 6, described between page 17, line 16, to page 18, line 28. The "means for detecting an address match condition ..." can be taken to include elements 509 and 521 as described on page 19, lines 17-22. The "means for outputting data ..." can be taken to include elements 515, 517, 519, and 525 of Figure 6, described between page 18, line 18, to page 20, line 2. The groups of memory cells storing data and addresses are shown in Figure 5. This figure shows an exemplary partition of memory sectors according to the present application. Figure 5 is primarily described beginning at line 23 of page 16. According to this sector partition, the sectors include a group of redundancy memory cells, 403 "DATA" or 407 "ALTERNATE DEFECTS DATA", that store data and a group of memory cells, 409 "DEFECT MAP", that store the addresses of defective cells and backup cells.

Claim 85 differs from claim 63 in that the preamble specifies a plurality of memory chips in addition to the defect management engine:

> 85. A defect management system comprising a plurality of memory chips, and at least one defect management engine chip coupled to each of said memory chips, said at least one defect management engine chip comprising:
>
> a memory array comprising a plurality of groups of data cells and address cells, said cells in each of said groups of data cells and address cells respectively storing data and addresses;
>
> means for accessing at least one of said plurality of groups of data cells and address cells;
>
> means for detecting an address match condition for each of said accessed groups, wherein the address of said accessed group matches an inputted address; and
>
> means for outputting data from said accessed group of data cells when said address match condition is detected.

The present patent application primarily describes this subject matter in the "Defect Mapping" section that begins on line 12 of page 14 of the specification. Figure 1B shows the controller 31, which has the defect management engine, and multiple EE PROM chips 43, 45, ..., 47. The various access, detection, and output circuit are shown for a read process in Figure 6, which is primarily described beginning on page 17, line 26. The "means for accessing ..." can be taken to include elements 503, 511, and 513 of Figure 6, described between page 17, line 16, to page 18,

line 28. The "means for detecting an address match condition ..." can be taken to include elements 509 and 521 as described on page 19, lines 17-22. The "means for outputting data ..." can be taken to include elements 515, 517, 519, and 525 of Figure 6, described between page 18, line 18, to page 20, line 2. The groups of memory cells storing data and addresses are shown in Figure 5. This figure shows an exemplary partition of memory sectors according to the present application. Figure 5 is primarily described beginning at line 23 of page 16. According to this sector partition, the sectors include a group of memory cells, 403 "DATA", that store data and a group of memory cells, 409 "DEFECT MAP", that store the addresses of defective cells and backup cells.

Claim 87 differs from claim 63 in that the preamble specifies a plurality of memory chips, each having a memory, in addition to the defect management engine:

> 87. A defect management system comprising a plurality of chips, each of said chips comprising at least one memory, and at least one defect management engine coupled to said at least one memory, said at least one defect management engine comprising: a memory array comprising a plurality of groups of data cells and address cells, said cells in each of said groups of data cells and address cells respectively storing data and addresses; means for accessing at least one of said plurality of groups of data cells and address cells; means for detecting an address match condition for each of said accessed groups, wherein the address of said accessed group matches an inputted address; and means for outputting data from said accessed group of data cells when said address match condition is detected.

The present patent application primarily describes this subject matter in the "Defect Mapping" section that begins on line 12 of page 14 of the specification. Figure 1B shows the controller 31, which has the defect management engine, and multiple EE PROM chips 43, 45, ..., 47. As shown in Figure 6, each chip has an array 33. The various access, detection, and output circuit are shown for a read process in Figure 6, which is primarily described beginning on page 17, line 26. The "means for accessing ..." can be taken to include elements 503, 511, and 513 of Figure 6, described between page 17, line 16, to page 18, line 28. The "means for detecting an address match condition ..." can be taken to include elements 509 and 521 as described on page 19, lines 17-22. The "means for outputting data ..." can be taken to include elements 515, 517, 519, and 525 of Figure 6, described between page 18, line 18, to page 20, line 2. The groups of memory cells storing data and addresses are shown in Figure 5. This figure shows an exemplary partition of memory sectors according to the present application. Figure 5 is primarily described beginning at line 23 of page 16. According to this sector partition, the sectors include a group of

memory cells, 403 "DATA", that store data and a group of memory cells, 409 "DEFECT MAP", that store the addresses of defective cells and backup cells.

Claim 89 differs from claim 63 in that the preamble specifies a plurality of memory chips, each having a memory, and a non-volatile random access memory in addition to the defect management engine:

> 89. A defect management system comprising a plurality of chips, each of said chips comprising at least one memory, at least one non-volatile random access memory coupled to said at least one memory, and at least one defect management engine coupled to said at least one memory, said at least one defect management engine comprising: a memory array comprising a plurality of groups of data cells and address cells said cells, in each of said groups of data cells and address cells respectively storing data and addresses; means for accessing at least one of said plurality of groups of data cells and address cells; means for detecting an address match condition for each of said accessed groups, wherein the address of said accessed group matches an inputted address; and means for outputting data from said accessed group of data cells when said address match condition is detected.

The present patent application primarily describes this subject matter in the "Defect Mapping" section that begins on line 12 of page 14 of the specification. Figure 1B shows the controller 31, which has the defect management engine, and multiple EE PROM chips 43, 45, ..., 47. As shown in Figure 6, each chip has an array 33. The non volatile random access memory be taken as any one of the EEPROM arrays. The various access, detection, and output circuit are shown for a read process in Figure 6, which is primarily described beginning on page 17, line 26. The "means for accessing ..." can be taken to include elements 503, 511, and 513 of Figure 6, described between page 17, line 16, to page 18, line 28. The "means for detecting an address match condition ..." can be taken to include elements 509 and 521 as described on page 19, lines 17-22. The "means for outputting data ..." can be taken to include elements 515, 517, 519, and 525 of Figure 6, described between page 18, line 18, to page 20, line 2. The groups of memory cells storing data and addresses are shown in Figure 5. This figure shows an exemplary partition of memory sectors according to the present application. Figure 5 is primarily described beginning at line 23 of page 16. According to this sector partition, the sectors include a group of memory cells, 403 "DATA", that store data and a group of memory cells, 409 "DEFECT MAP", that store the addresses of defective cells and backup cells.

Claim 91 is a method counterpart of claim 63:

> 91. A method of managing defects comprising the steps of:

configuring a memory array in a plurality of groups of data cells and address cells, said cells in each of said groups of data cells and address cells respectively storing data and addresses;

accessing at least one of said plurality of groups of data cells and address cells;

detecting an address match condition for each of said accessed groups, wherein the address of said accessed group matches one of a plurality of inputted addresses; and

outputting data from said accessed group of data cells and address cells when said address match condition is detected.

The present patent application primarily describes this subject matter in the "Defect Mapping" section that begins on line 12 of page 14 of the specification. The various access, detection, and output circuit are shown for a read process in Figure 6, which is primarily described beginning on page 17, line 26. The "accessing ..." can be taken to include elements 503, 511, and 513 of Figure 6, described between page 17, line 16, to page 18, line 28. The "detecting an address match condition ..." can be taken to include elements 509 and 521 as described on page 19, lines 17-22. The "outputting data ..." can be taken to include elements 515, 517, 519, and 525 of Figure 6, described between page 18, line 18, to page 20, line 2. The groups of memory cells storing data and addresses are shown in Figure 5. This figure shows an exemplary partition of memory sectors according to the present application. Figure 5 is primarily described beginning at line 23 of page 16. According to this sector partition, the sectors include a group of memory cells, 403 "DATA", that store data and a group of memory cells, 409 "DEFECT MAP", that store the addresses of defective cells and backup cells.

Claim 96 is a method counterpart of claim 82:

96. A method of managing defects comprising the steps of:

configuring a memory array into a plurality of groups of redundancy data cells and redundancy address cells, said cells respectively storing redundancy data and redundancy addresses;

accessing at least one of said plurality of groups of redundancy data cells and redundancy address cells;

detecting a redundancy address match condition for each of said accessed groups, wherein the redundancy address of said accessed group of redundancy address cells matches one of a plurality of inputted addresses; and

outputting redundancy data from said accessed group of redundancy data cells and redundancy address cells when said redundancy address match condition is detected.

The present patent application primarily describes this subject matter in the "Defect Mapping" section that begins on line 12 of page 14 of the specification. The various access, detection, and output circuit are shown for a read process in Figure 6, which is primarily described beginning on page 17, line 26. The "accessing ..." can be taken to include elements 503, 511, and 513 of

Figure 6, described between page 17, line 16, to page 18, line 28. The "detecting an address match condition ..." can be taken to include elements 509 and 521 as described on page 19, lines 17-22. The "outputting data ..." can be taken to include elements 515, 517, 519, and 525 of Figure 6, described between page 18, line 18, to page 20, line 2. The groups of memory cells storing data and addresses are shown in Figure 5. This figure shows an exemplary partition of memory sectors according to the present application. Figure 5 is primarily described beginning at line 23 of page 16. According to this sector partition, the sectors include a group of redundancy memory cells, 403 "DATA" or 407 "ALTERNATE DEFECTS DATA", that store data and a group of memory cells, 409 "DEFECT MAP", that store the addresses of defective cells and backup cells.

Claim 98 uses the "first cells" and "second cells" language:

> 98. A defect management engine comprising:
> a memory array comprising a plurality of groups of first cells and second cells, said cells in each of said groups of first cells and second cells respectively storing data and addresses;
> means for accessing at least one of said plurality of groups of first cells and second cells;
> means for detecting an address match condition for each of said accessed groups, wherein the address of said accessed group matches an inputted address; and
> means for outputting data from said accessed group of first cells when said address match condition is detected.

The present patent application primarily describes this subject matter in the "Defect Mapping" section that begins on line 12 of page 14 of the specification. The various access, detection, and output circuit are shown for a read process in Figure 6, which is primarily described beginning on page 17, line 26. The "means for accessing ..." can be taken to include elements 503, 511, and 513 of Figure 6, described between page 17, line 16, to page 18, line 28. The "means for detecting an address match condition ..." can be taken to include elements 509 and 521 as described on page 19, lines 17-22. The "means for outputting data ..." can be taken to include elements 515, 517, 519, and 525 of Figure 6, described between page 18, line 18, to page 20, line 2. The groups of memory cells storing data and addresses are shown in Figure 5. This figure shows an exemplary partition of memory sectors according to the present application. Figure 5 is primarily described beginning at line 23 of page 16. According to this sector partition, the sectors include a first group of memory cells, 403 "DATA", that store data and a

second group of memory cells, 409 "DEFECT MAP", that store the addresses of defective cells and backup cells.

Claim 99 adds to claim 98 that the defect management engine in coupled to "at least on main memory" and in that the "address cells" and "memory cells" store "redundancy data" and "redundancy addresses":

> 99. A defect management engine coupled to at least one main memory comprising:
>
> a memory array comprising a plurality of groups of first cells and second cells, said cells in each of said groups of first cells and second cells respectively storing backup data and backup addresses;
>
> means for accessing at least one of said plurality of groups of first cells and second cells;
>
> means for detecting a backup address match condition for each of said accessed groups, wherein the backup address of said accessed group matches one of a plurality of inputted addresses; and
>
> means for outputting backup data from said accessed group of first cells and second cells when said backup address match condition is detected.

The present patent application primarily describes this subject matter in the "Defect Mapping" section that begins on line 12 of page 14 of the specification. The defect management engine is part of controller 31 in Figure 6, with the memory as 33. The various access, detection, and output circuit are shown for a read process in Figure 6, which is primarily described beginning on page 17, line 26. The "means for accessing ..." can be taken to include elements 503, 511, and 513 of Figure 6, described between page 17, line 16, to page 18, line 28. The "means for detecting an address match condition ..." can be taken to include elements 509 and 521 as described on page 19, lines 17-22. The "means for outputting data ..." can be taken to include elements 515, 517, 519, and 525 of Figure 6, described between page 18, line 18, to page 20, line 2. The groups of memory cells storing data and addresses are shown in Figure 5. This figure shows an exemplary partition of memory sectors according to the present application. Figure 5 is primarily described beginning at line 23 of page 16. According to this sector partition, the sectors include a group of redundancy memory cells, 403 "DATA" or 407 "ALTERNATE DEFECTS DATA", that store data and a group of memory cells, 409 "DEFECT MAP", that store the addresses of defective cells and backup cells.

Claim 100 differs from claim 98 in that the preamble specifies a plurality of memory chips in addition to the defect management engine:

100. A defect management system comprising a plurality of memory chips, and at least one defect management engine chip coupled to each of said memory chips, said at least one defect management engine chip comprising:

a memory array comprising a plurality of groups of first cells and second cells, said cells in each of said groups of first cells and second cells respectively storing data and addresses;

means for accessing at least one of said plurality of groups of first cells and second cells;

means for detecting an address match condition for each of said accessed groups, wherein the address of said accessed group matches an inputted address; and

means for outputting data from said accessed group of first cells when said address match condition is detected.

The present patent application primarily describes this subject matter in the "Defect Mapping" section that begins on line 12 of page 14 of the specification. Figure 1B shows the controller 31, which has the defect management engine, and multiple EE PROM chips 43, 45, ..., 47. The various access, detection, and output circuit are shown for a read process in Figure 6, which is primarily described beginning on page 17, line 26. The "means for accessing ..." can be taken to include elements 503, 511, and 513 of Figure 6, described between page 17, line 16, to page 18, line 28. The "means for detecting an address match condition ..." can be taken to include elements 509 and 521 as described on page 19, lines 17-22. The "means for outputting data ..." can be taken to include elements 515, 517, 519, and 525 of Figure 6, described between page 18, line 18, to page 20, line 2. The groups of memory cells storing data and addresses are shown in Figure 5. This figure shows an exemplary partition of memory sectors according to the present application. Figure 5 is primarily described beginning at line 23 of page 16. According to this sector partition, the sectors include a group of memory cells, 403 "DATA", that store data and a group of memory cells, 409 "DEFECT MAP", that store the addresses of defective cells and backup cells.

Claim 101 differs from claim 98 in that the preamble specifies a plurality of memory chips, each having a memory, in addition to the defect management engine:

101. A defect management system comprising a plurality of chips, each of said chips comprising at least one memory, and at least one defect management engine coupled to said at least one memory, said at least one defect management engine comprising: a memory array comprising a plurality of groups of first cells and second cells, said cells in each of said groups of first cells and second cells respectively storing data and addresses; means for accessing at least one of said plurality of groups of first cells and second cells; means for detecting an address match condition for each of said accessed groups, wherein the address of said accessed group matches an inputted address;

and means for outputting data from said accessed group of first cells when said address match condition is detected.

The present patent application primarily describes this subject matter in the "Defect Mapping" section that begins on line 12 of page 14 of the specification. Figure 1B shows the controller 31, which has the defect management engine, and multiple EE PROM chips 43, 45, ..., 47. As shown in Figure 6, each chip has an array 33. The various access, detection, and output circuit are shown for a read process in Figure 6, which is primarily described beginning on page 17, line 26. The "means for accessing ..." can be taken to include elements 503, 511, and 513 of Figure 6, described between page 17, line 16, to page 18, line 28. The "means for detecting an address match condition ..." can be taken to include elements 509 and 521 as described on page 19, lines 17-22. The "means for outputting data ..." can be taken to include elements 515, 517, 519, and 525 of Figure 6, described between page 18, line 18, to page 20, line 2. The groups of memory cells storing data and addresses are shown in Figure 5. This figure shows an exemplary partition of memory sectors according to the present application. Figure 5 is primarily described beginning at line 23 of page 16. According to this sector partition, the sectors include a group of memory cells, 403 "DATA", that store data and a group of memory cells, 409 "DEFECT MAP", that store the addresses of defective cells and backup cells.

Claim 102 is a method counterpart of claim 98:

102. A method of managing defects comprising the steps of:

configuring a memory array in a plurality of groups of first cells and second cells, said cells in each of said groups of first cells and second cells respectively storing data and addresses;

accessing at least one of said plurality of groups of first cells and second cells;

detecting an address match condition for each of said accessed groups, wherein the address of said accessed group matches one of a plurality of inputted addresses; and

outputting data from said accessed group of first cells and second cells when said address match condition is detected.

The present patent application primarily describes this subject matter in the "Defect Mapping" section that begins on line 12 of page 14 of the specification. The various access, detection, and output circuit are shown for a read process in Figure 6, which is primarily described beginning on page 17, line 26. The "accessing ..." can be taken to include elements 503, 511, and 513 of Figure 6, described between page 17, line 16, to page 18, line 28. The "detecting an address match condition ..." can be taken to include elements 509 and 521 as described on page 19, lines 17-22. The "outputting data ..." can be taken to include elements 515, 517, 519, and 525 of

Figure 6, described between page 18, line 18, to page 20, line 2. The groups of memory cells storing data and addresses are shown in Figure 5. This figure shows an exemplary partition of memory sectors according to the present application. Figure 5 is primarily described beginning at line 23 of page 16. According to this sector partition, the sectors include a group of memory cells, 403 "DATA", that store data and a group of memory cells, 409 "DEFECT MAP", that store the addresses of defective cells and backup cells.

Claim 103 is a method counterpart of claim 99:

> 103. A method of managing defects comprising the steps of:
> configuring a memory array into a plurality of groups of first cells and second cells, said cells respectively storing backup data and backup addresses;
> accessing at least one of said plurality of groups of first cells and second cells;
> detecting a backup address match condition for each of said accessed groups, wherein the backup address of said accessed group of second cells matches one of a plurality of inputted addresses; and
> outputting backup data from said accessed group of first cells and second cells when said backup address match condition is detected.

The present patent application primarily describes this subject matter in the "Defect Mapping" section that begins on line 12 of page 14 of the specification. The various access, detection, and output circuit are shown for a read process in Figure 6, which is primarily described beginning on page 17, line 26. The "accessing ..." can be taken to include elements 503, 511, and 513 of Figure 6, described between page 17, line 16, to page 18, line 28. The "detecting an address match condition ..." can be taken to include elements 509 and 521 as described on page 19, lines 17-22. The "outputting data ..." can be taken to include elements 515, 517, 519, and 525 of Figure 6, described between page 18, line 18, to page 20, line 2. The groups of memory cells storing data and addresses are shown in Figure 5. This figure shows an exemplary partition of memory sectors according to the present application. Figure 5 is primarily described beginning at line 23 of page 16. According to this sector partition, the sectors include a group of redundancy memory cells, 403 "DATA" or 407 "ALTERNATE DEFECTS DATA", that store data and a group of memory cells, 409 "DEFECT MAP", that store the addresses of defective cells and backup cells.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The Board is asked to review the correctness of the rejections under 35 U.S.C. §112, first paragraph. Specifically, claims 63-103 stand rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement. The Office Action alleges that "the specification fails to describe groups of address cells for storing address[es] in a memory array." This is the basis for rejecting all of the independent claims and is the sole issue in this appeal. All of the claims can be taken to form a single group, with independent claim 98 suitable for deciding whether the group of claims is patentable.

VII. ARGUMENT

The most recent Office Action, from which this Appeal originates, rejects all of the pending claims under 35 U.S.C. §112, first paragraph, for failing to comply with the written description requirement. All of these claims are rejected on the same ground, namely a lack of written description for "a memory array comprising a plurality of groups of ... address cells, said cells in each of said groups of ... address cells ... storing ... addresses", where this or a similar limitation is found in all of the independent claims. Consequently, all of the claims are argued together and, when reference to a specific claim is required, claim 98 is believed suitable for this purpose.

Claim 98 begins:

> 98. A defect management engine comprising:
> a memory array comprising a plurality of groups of first cells and second cells, said cells in each of said groups of first cells and second cells respectively storing data and addresses;

where support for support for "a plurality of groups of first cells ..., said cells in each of said groups of first cells ... storing data" is not questioned. It is on "a plurality of groups of ... second cells, said cells in each of said groups of ... second cells ... storing ... addresses" that the Office Action bases its rejection.

Figure 5, as described primarily between line 23 of page 16 and line 25 of page 17, shows a typical memory sector 401 whose cells are organized into a data portion 403 and a "spare portion" 405. (The "cells ... storing data" correspond to DATA 403 and can also be taken to include ALTERNATE DEFECTS DATA 407.) The cells of the "spare portion" are further

organized to include a "defect map area" 409. As stated at page 17, lines 6-8: "The **addresses** of the defective cell **are stored** as defect pointers **in the defect map 409**." Thus, as the added emphasis shows, there is clear disclosure of a group of cells storing addresses. As there are a plurality of such sectors (see, e.g., Figure 2 or Figure 3A), there are a corresponding plurality such groups. Consequently, it is believed that the present application clearly provides suitable written description of "a plurality of groups of ... cells ... storing ... addresses" and that the rejection under 35 U.S.C. §112, first paragraph, is not well founded.

In its Response to Arguments section, the Office Action from which this Appeal originates states (page 3, last paragraph):

> At the bottom of page 11 and on page 12 [of the last Amendment], the Applicants again argued that the present application provides support for "address cells ... storing ... addresses". On the contrary, the specification on page 17, lines 6-8, only describes the addresses of the defective cell and the backup cell stored as defect pointers in the defect map 409.

The emphasis and ellipses are in the original. From the last sentence in this quote, the Office Action admits that the specification "describes the addresses ... stored" in the memory cells of "the defect map"; but, rather, the Office Action seems to be basing its rejection on this support stating that these addresses are stored in the form of "defect pointers"; that is, the Office Action is rejecting the claims *not* based on a lack of support *for the claim element itself*, but is instead basing it on some further requirement *not found in the claim itself*. (As for the "defect" part of "defect pointers", it should be noted that the preamble explicitly states that the claim is for a "defect management engine"; thus, the substance of the rejection appears to be based on an objection to the *form* in which the addresses being stored ("pointers"), a limitation not found in the claims.)

Based on these comments, the Office Action seems to be requiring that present application provide not just support for the claims as written, but for a specific embodiment–or, perhaps more accurately, seems to require support for ruling out a particular embodiment. This is improper. The correct question is whether the present specification is enabling for the claims ***as written***. The claims contain ***no such limiting language*** (such as "wherein said addresses are not stored as pointers" or other such limiting language) that would restrict that would restrict them in this way. As noted in 37 CFR 41.200(b), "[a] claim shall be given it broadest reasonable construction. ...". Similarly, as noted in the M.P.E.P.§2111, claims must be given their broadest

reasonable interpretation; in contrast, the Office Action appears to be reading limitations into the claim that are not there and then improperly issuing a rejection on this basis. As noted above, support for the disputed claim element *as written* is explicitly given at page 17, lines 6-8 of the specification: "The addresses ... are stored ... defect map".

(As noted above in Section III above, the currently pending claims in the present application are either copied from, or correspond to claims found in U.S. patent 6,141,267. Although not explicitly stated in the Office Actions, it may be that the Office Action is requiring that present application provide not just support for the claims as written, but for a specific embodiment of U.S. patent 6,141,267. (This mistake was explicitly made in the first Office Action for the present application, see the Office Action mailed January 31, 2003, last paragraph beginning on page 2.) This is again improper and the correct question is whether the present specification is enabling for the claim ***as written***.)

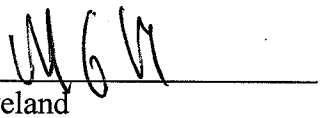
Consequently, for any of these reasons, it is respectfully submitted that the rejection of claims 63-103 under the first paragraph of 35 U.S.C. §112 is not well founded and should be withdrawn. As described above, the specification is believed to more than satisfy the written description require for "a memory array comprising a plurality of groups of first cells and second cells, said cells in each of said groups of first cells and second cells respectively storing data and addresses".

VIII. CONCLUSION

It is Applicants' position, as indicated above, that the assertions of the Office Action are incorrect. The subject matter of the claims is provided with an adequate written description by

the subject application. Accordingly, the rejection of the application should be reversed and the present patent application passed to issue.

Respectfully submitted,



3-18-2008

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Appendix A

CLAIMS PENDING IN APPLICATION SERIAL NO. 10/000,155

Claims 1-62 are cancelled.

63. A defect management engine comprising:

a memory array comprising a plurality of groups of data cells and address cells, said cells in each of said groups of data cells and address cells respectively storing data and addresses;

means for accessing at least one of said plurality of groups of data cells and address cells;

means for detecting an address match condition for each of said accessed groups, wherein the address of said accessed group matches an inputted address; and

means for outputting data from said accessed group of data cells when said address match condition is detected.

64. The defect management engine as recited in claim 63, further comprising at least one main memory wherein said data cells are redundancy data cells for replacing defective ones of said data cells in said at least one main memory, and said address cells are redundancy address cells for storing addresses of defective ones of data cells in said at least one main memory.

65. The defect management engine as recited in claim 63 further comprising means for overriding said accessed group of data cells respectively with new data, when said address match condition is detected

66. The defect management engine as recited in claim 63, wherein said data cells and said address cells are of a same cell type.

67. The defect management engine as recited in claim 63, wherein addresses stored in said address cells are non-volatile.

68. The defect management engine as recited in claim 63 further comprising means for programming addresses stored in said address cells.

69. The defect management engine recited in claim 64, wherein said redundancy data cells are of a same cell type as said data cells in said at least one main memory

70. The defect management engine as recited in claim 68, wherein said means for programming is enabled by a command generated by a controller means.

71. The defect management engine as recited in claim 68, wherein said means for programming replicates said addresses into said address cells by sequentially activating each of said address cells.

72. The defect management engine as recited in claim 68, wherein said means for programming replicates said addresses into said address cells by simultaneously activating at least two of said address cells.

73. The defect management engine as recited in claim 64 further comprising means for enabling a single-bit and a multi-bit redundancy replacement within said at least one main memory.

74. The defect management engine as recited in claim 73, wherein said multi-bit size redundancies replace multiple defective ones of said data cells within said at least one main memory with one group of said plurality of groups of redundancy data cells

75. The defect management engine as recited in claim 73 further comprising means for enabling a variable bit size redundancy replacement in said at least one main memory.

76. The defect management engine as recited in claim 64, wherein said data cells are redundancy data cells for replacing defective ones of said data cells present in at least one domain within said at least one main memory, and said address cells are redundancy address cells for addressing defective ones of said data cells within said at least one domain.

77. The defect management engine as recited in claim 76, wherein said plurality of groups of redundancy data cells and redundancy address cells is assigned to said at least one domain.

78. The defect management engine as recited in claim 76, wherein said at least one domain within said at least one main memory is supported by at least one of said plurality of groups of redundancy data cells and redundancy address cells.

79. The defect management engine as recited in claim 63, wherein said means for accessing at least one of said plurality of groups includes wordline drivers.

80. The defect management engine as recited in claim 79, wherein said means for accessing at least one of said plurality of groups further includes sense amplifiers.

81. The defect management engine as recited in claim 79, wherein said wordline driver enables means for assigning to said plurality of groups of data cells and address cells respective redundancy ones of said redundancy data cells and redundancy address cells to repair a plurality of faults in at least one of said domains.

82. A defect management engine coupled to at least one main memory comprising:

a memory array comprising a plurality of groups of redundancy data cells and redundancy address cells, said cells in each of said groups of redundancy data cells and redundancy address cells respectively storing redundancy data and redundancy addresses;

means for accessing at least one of said plurality of groups of redundancy data cells and redundancy address cells;

means for detecting a redundancy address match condition for each of said accessed groups, wherein the redundancy address of said accessed group matches one of a plurality of inputted addresses; and

means for outputting redundancy data from said accessed group of redundancy data cells and redundancy address cells when said redundancy address match condition is detected.

83. The defect management engine as recited in claim 82 further comprising means for overriding said accessed group of redundancy data cells with new data when said redundancy address match condition is detected.

84. The defect management engine as recited in claim 82, wherein said redundancy data cells and said redundancy address cells are of a same cell type

85. A defect management system comprising a plurality of memory chips, and at least one defect management engine chip coupled to each of said memory chips, said at least one defect management engine chip comprising:

a memory array comprising a plurality of groups of data cells and address cells, said cells in each of said groups of data cells and address cells respectively storing data and addresses;

means for accessing at least one of said plurality of groups of data cells and address cells;

means for detecting an address match condition for each of said accessed groups, wherein the address of said accessed group matches an inputted address; and

means for outputting data from said accessed group of data cells when said address match condition is detected.

86. The defect management system as recited in claim 85 further comprising a non-volatile random access memory chip coupled to each of said memory chips.

87. A defect management system comprising a plurality of chips, each of said chips comprising at least one memory, and at least one defect management engine coupled to said at least one memory, said at least one defect management engine comprising: a memory array comprising a plurality of groups of data cells and address cells, said cells in each of said groups of data cells and address cells respectively storing data and addresses; means for accessing at least one of said plurality of groups of data cells and address cells; means for detecting an

address match condition for each of said accessed groups, wherein the address of said accessed group matches an inputted address; and means for outputting data from said accessed group of data cells when said address match condition is detected.

88. The defect management system as recited in claim 87 further comprising at least one non-volatile random access memory coupled to said at least one memory and to said at least one defect management engine.

89. A defect management system comprising a plurality of chips, each of said chips comprising at least one memory, at least one non-volatile random access memory coupled to said at least one memory, and at least one defect management engine coupled to said at least one memory, said at least one defect management engine comprising: a memory array comprising a plurality of groups of data cells and address cells said cells, in each of said groups of data cells and address cells respectively storing data and addresses; means for accessing at least one of said plurality of groups of data cells and address cells; means for detecting an address match condition for each of said accessed groups, wherein the address of said accessed group matches an inputted address; and means for outputting data from said accessed group of data cells when said address match condition is detected.

90. The defect management system as recited in claim 89 further comprising at least one defect management engine chip coupled to each of said chips comprising said at least one memory and to said at least one non-volatile random access memory.

91. A method of managing defects comprising the steps of:

configuring a memory array in a plurality of groups of data cells and address cells, said cells in each of said groups of data cells and address cells respectively storing data and addresses;

accessing at least one of said plurality of groups of data cells and address cells;

detecting an address match condition for each of said accessed groups, wherein the address of said accessed group matches one of a plurality of inputted addresses; and

outputting data from said accessed group of data cells and address cells when said address match condition is detected.

92. The method of managing defects as recited in claim 91 further comprising the step of overriding with new data said accessed group of data cells when said address match condition is detected.

93. The method of managing defects as recited in claim 91, wherein said data cells and said address cells are of a same cell type.

94. The method of managing defects as recited in claim 91, wherein the addresses stored in said address cells are non-volatile.

95. The method of managing defects as recited in claim 91 further comprising means for programming said addresses stored in at least one of said address cells.

96. A method of managing defects comprising the steps of:

configuring a memory array into a plurality of groups of redundancy data cells and redundancy address cells, said cells respectively storing redundancy data and redundancy addresses;

accessing at least one of said plurality of groups of redundancy data cells and redundancy address cells;

detecting a redundancy address match condition for each of said accessed groups, wherein the redundancy address of said accessed group of redundancy address cells matches one of a plurality of inputted addresses; and

outputting redundancy data from said accessed group of redundancy data cells and redundancy address cells when said redundancy address match condition is detected.

97. The defect management engine as recited in claim 96 further comprising the step of overriding with new data said accessed group of redundancy data cells when said redundancy address match condition is detected.

98. A defect management engine comprising:

a memory array comprising a plurality of groups of first cells and second cells, said cells in each of said groups of first cells and second cells respectively storing data and addresses;

means for accessing at least one of said plurality of groups of first cells and second cells;

means for detecting an address match condition for each of said accessed groups, wherein the address of said accessed group matches an inputted address; and

means for outputting data from said accessed group of first cells when said address match condition is detected.

99. A defect management engine coupled to at least one main memory comprising:

a memory array comprising a plurality of groups of first cells and second cells, said cells in each of said groups of first cells and second cells respectively storing backup data and backup addresses;

means for accessing at least one of said plurality of groups of first cells and second cells;

means for detecting a backup address match condition for each of said accessed groups, wherein the backup address of said accessed group matches one of a plurality of inputted addresses; and

means for outputting backup data from said accessed group of first cells and second cells when said backup address match condition is detected.

100. A defect management system comprising a plurality of memory chips, and at least one defect management engine chip coupled to each of said memory chips, said at least one defect management engine chip comprising:

a memory array comprising a plurality of groups of first cells and second cells, said cells in each of said groups of first cells and second cells respectively storing data and addresses;

means for accessing at least one of said plurality of groups of first cells and second cells;

means for detecting an address match condition for each of said accessed groups, wherein the address of said accessed group matches an inputted address; and

means for outputting data from said accessed group of first cells when said address match condition is detected.

101. A defect management system comprising a plurality of chips, each of said chips comprising at least one memory, and at least one defect management engine coupled to said at least one memory, said at least one defect management engine comprising: a memory array comprising a plurality of groups of first cells and second cells, said cells in each of said groups of first cells and second cells respectively storing data and addresses; means for accessing at least one of said plurality of groups of first cells and second cells; means for detecting an address match condition for each of said accessed groups, wherein the address of said accessed group matches an inputted address; and means for outputting data from said accessed group of first cells when said address match condition is detected.

102. A method of managing defects comprising the steps of:

configuring a memory array in a plurality of groups of first cells and second cells, said cells in each of said groups of first cells and second cells respectively storing data and addresses;

accessing at least one of said plurality of groups of first cells and second cells;

detecting an address match condition for each of said accessed groups, wherein the address of said accessed group matches one of a plurality of inputted addresses; and

outputting data from said accessed group of first cells and second cells when said address match condition is detected.

103. A method of managing defects comprising the steps of:

configuring a memory array into a plurality of groups of first cells and second cells, said cells respectively storing backup data and backup addresses;

accessing at least one of said plurality of groups of first cells and second cells;

detecting a backup address match condition for each of said accessed groups, wherein the backup address of said accessed group of second cells matches one of a plurality of inputted addresses; and

outputting backup data from said accessed group of first cells and second cells when said backup address match condition is detected.

X. EVIDENCE APPENDIX

None.

XI. RELATED PROCEEDINGS APPENDIX

DECISION ON PRELIMINARY MOTIONS
PATENT INTERFERENCE NO. 104,760

DECISION ON YAMAGAMI SECOND REQUEST FOR RECONSIDERATION AND FINAL JUDGMENT, PATENT INTERFERENCE NO. 104,760

DECISION ON APPEAL, APPEAL NO. 2001-1272

U.S. INTERNATIONAL TRADE COMMISSION, INVESTIGATION NO. 337-TA-382

U.S. INTERNATIONAL TRADE COMMISSION, INVESTIGATION NO. 337-TA-560

DECISION ON APPEAL, *SANDISK CORPORATION V. MEMOREX PRODUCTS, INC.*, 415 F.3D 1278, 75USPQ 2D1475 (FED. CIR. 2005)